On the Origin of Coercive Voltage Enhancement in Ferroelectric-Dielectric Heterostructures for Ferroelectric NAND Applications

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Charge-trap Flash (CTF) technology faces significant challenges in retention at reduced z-pitches due to lateral charge migration [1]. Ferroelectric (FE)-NAND has emerged as a potential alternative to CTF-NAND due to its scalability, higher operating speeds, and low operating voltages. However, the memory window (MW) in standard FE field effect transistors is dependent on the coercive voltage ($2V_C$), which is often limited to 4 V at 3D NAND compatible thicknesses. It was shown that inserting a dielectric (DE) into the FE stack can boost the V_C by multiple folds [2][3]. However, the origin of this enhancement remains widely debated. We propose that the mechanism behind V_C enhancement is directly linked to the leakage in the FE and DE layers. Using preisach model-based simulations with external leaky capacitors, we show that the V_C increases as the leakage through the DE decreases. Importantly, we attribute the increase in V_C to the resistive voltage division between the FE and DE layers. Fig 1(a) shows a standard FE (19 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO)) and FE-DE heterostructures with a tunnel dielectric layer (TDL) (9.5 HZO/1 Al_2O_3/9.5 HZO and 8.5 HZO/3 Al_2O_3/ 8.5 HZO) and gate blocking layer (GBL) (19 HZO/1 Al_2O_3). Fig 1(b) shows the polarization-voltage (P-V) loop for all 4 structures. 19 HZO has a $2V_C$ of about 3.6 V. The structures with a dielectric insert boast a V_C increase over 2x.

Here, we model these gate stacks as individual leaky capacitors connected in series. The ferroelectric layers are modeled by a non-linear capacitor (C_{FE}) with a resistor (R_{FE}) in parallel to simulate leakage. The dielectric inserts are modeled similarly as a linear capacitor (C_{DE}) with a resistor (R_{DE}) in parallel. We model the FE-DE interface as an equipotential surface [4]. From this model, the effective V_C of the heterogeneous structures is given as,

$$V_C = (1 + \frac{R_{DE}}{R_{FE}}) \cdot V_{C,0}$$

Using devices simulations, we study the voltage across the individual layers. Fig. 2(a&b) shows the P-V and current-voltage (I-V) of a standard FE stack (17 nm HZO) with R_{FE}=350 kΩ simulated using a Preisach model [5]. Fig. 2(c&d) shows the P-V and I-V loops for a FE-DE heterostructure with a 3 nm Al_2O_3 insert with R_{DE}=870 kΩ to simulate the leaky dielectric. Fig. 3(e) shows the effect of R_{DE} on the voltage division between the layers and intrinsic V_C of the FE layer showing that the V_C increase originates due to voltage division between the layers.

References

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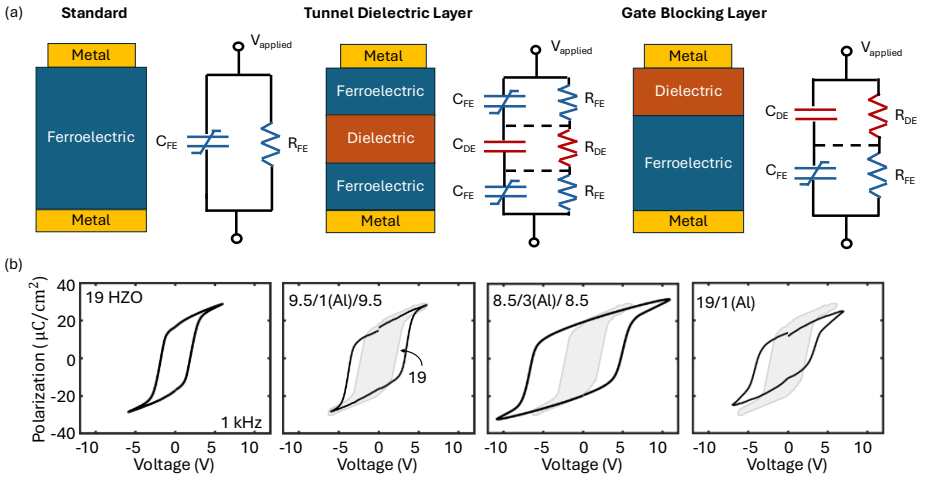

Figure 1. Dielectric inserts in ferroelectric gate stacks lead to an enhanced coercive voltage ($2V_C$) (a)The two common types of dielectric inserts are Tunnel Dielectric layer (TDL), where the dielectric is in the middle of the ferroelectric stack, and Gate Blocking Layer (GBL), where the ferroelectric stack is between the ferroelectric and electrode. (b) The polarization-voltage (P-V) loops of a TDL and GBL structure show a larger $2V_C$ compared to that of a standard structure.

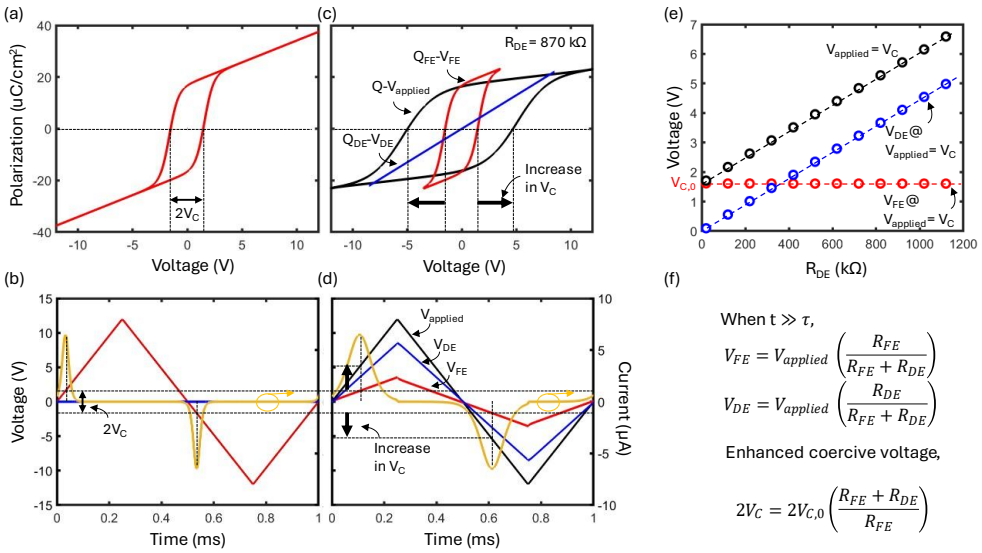

Figure 2. Simulated P-V characteristics of (a) stand-alone 17 nm HZO and (c) leaky FE-DE heterostructure with R_{DE} = 870 kΩ, R_{FE} = 350 kΩ and C_{DE} equivalent to that of a 3 nm Al_2O_3 layer. The heterostructure exhibits more than twice the coercive voltage of the standalone HZO. The voltage across different layers and the switching current for both cases are shown in (b) and (d), respectively. It is observed in (e) that the voltage division between the ferroelectric and dielectric layers are governed by the leakage resistors. This voltage division can be modeled and used to find the new $2V_C$ in the functions seen in (f).